AMENDMENTS TO THE SPECIFICATION:

Please amend the paragraph beginning at page 10, line 25, and continuing to page 11, line 15, as follows:

As shown in more detail in Fig. 4A, the input/output unit 247 includes a channel switching unit 300 and a processor herein known as packet reception rate analyzer 301. ATM cells from switch 240 are applied to an appropriate one of plural buffers 304_a - 304_n in input/output unit 247. Buffer 304_a is employed for a first active session; buffer 304_n is employed for an n^{th} active session, it being understood from Fig. 4A that unillustrated buffers a+1 through n-1 are also provided for respective sessions a+1 through n-1. The packet reception rate analyzer 301 is connected to analyze the rate of reception of data packets in each of in buffers 304, and to apply switch control information to a corresponding one of switch control units 307_a - 307_n. The switch control units 307_a - 307_n control demuliplexing of data packets (via respective demultiplexers 308) out of buffers 304. Multiplexers 308 are controlled by switch control units 307 for applying data packets either to respective common channel output buffers 310 or to respective dedicated channel output buffers 312. Thus the switch control units 307_x control multiplexers 308_x (x = a,... n) for routing of data packets to one of common channel output buffer 310_x or to dedicated channel output buffer 312_x. The buffers 304 and 310, 312 are FIFO buffers. The outputs of buffers 312_x ~~being~~ are applied to switch 240. The outputs of buffers 310_x are applied to inputs of demultiplexer 315. Under supervision of switch control 307_{CC} the demultiplexer 315 routes data packets onto a common port of switch 240. Thus, the packet reception rate analyzer 301, the switch control units 307, multiplexers 308, demultiplexer 315, and the buffers 310 and 312 comprise the channel switching unit 300. In channel switching unit 300, the packet reception rate analyzer 301 and the various switch controls operate under supervision of an unillustrated master controller which, e.g., sequences and coordinates operation.

Please amend the paragraph beginning at page 14, line 21, and continuing to page 14, line 29, as follows:

If it is determined at step 6-3 that a channel type switch is to be invoked, a channel type switch occurs at step 6-6. Assuming that the session had previously employed a common channel, at step 6-6 a dedicated channel is allocated to the data packet transaction session. In addition, in connection with the channel type switch the routing of data packets of the session is changed from the common channel (CC) output buffer to the dedicated channel (DC) output buffer for the allocated dedicated channel. Such routing switch of packets is illustrated in Fig. 4A by switch control unit 307 controlling the multiplexer 308 so that the data packets are routed to the dedicated channel (DC) output buffer 312 rather than the common channel (CC) output buffer 310.

a2